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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,291	04/13/2004	Hidehiko Suzuki	08211/0200655-US0/P05800	4557

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EXAMINER	
HILTUNEN, THOMAS J	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/823,291	SUZUKI, HIDEHIKO	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☒ Claim(s) 8 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/20/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of the following informalities: Claim 8 appears to be missing a word. It is believed the word "with" was intended to be in between the words "associated" and "the" as in claim 15, and has been treated as such for the remainder of this office action. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kong et al. (USPN 6,242,973).

With respect to claim 1, Kong et al. discloses, in Fig.2, a circuit comprising: "a logic circuit (M1 and M2) including a p-type transistor (M1) and an n-type transistor (M2)"; and "a voltage offset circuit (remainder of circuit) that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that

the second voltage is positively offset relative to the first voltage". Kong et al. discloses a voltage offset through using bootstrap capacitors Cp and Cn. First the capacitor Cp and Cn create a boosted effective control signal opposite in polarity. Additionally in both situations of a high or low input (IN) voltage, M2's gate voltage is positively offset to that of M1's. (See Kong et al. col.2 lines 15-67 and col. 3 lines 1-30.)

With respect to claim 2, "the logic circuit is arranged as an inverter circuit (element 11 of Fig.2)".

With respect to claim 3, the definition of the term "resistor" includes "A device used to control current in an electric circuit by providing resistance" (The American Heritage Dictionary of the English Language, Fourth Edition, 2000). Almost every component in a circuit provides a resistance that limits current, therefore it is reasonable to interpret capacitors Cp and Cn, or even any of the transistors in circuit 10 of Fig. 2 as resistors.

With respect to claim 4, the capacitors Cp and Cn are arranged serially.

With respect to claim 5, the recited "capacitor circuit" would read on capacitors Cp and Cn.

With respect to claim 6, capacitors Cp and Cn are serially connected.

With respect to claim 7, the bootstrapped configuration of Cp and Cn in Fig. 2 creates a larger effective supply voltage.

With respect to claim 8, the increase in "operation speed" discussed in lines 21-30 of col. 1 of Kong et al. will inherently provide the recited operation of reduced propagation delay.

With respect to claim 9, transistors M3 and M8, being connected to a supply voltage and ground, clearly provide a current source for circuit 10.

With respect to claim 10, it is well know in the art that the switching of current through a capacitor causes a voltage ramp. This is situation is disclosed in Kong et al., when the voltage supply changes from a high to low value. This causes capacitor Cp in Fig. 2 to become a voltage ramp that differs from the voltage ramp that would occur in Cn, as they would be opposite in magnitude.

With respect to claim 11, Kong et al. discloses in Fig. 2 a circuit comprising: "a current source circuit that is configured to provide a current (M3 and M8); "a capacitor circuit that is configured to provide a first voltage in response to the current (capacitors Cp and Cn)"; "a voltage offset circuit that is coupled between the current circuit and the capacitor circuit, wherein the voltage offset circuit is arranged to provide a second voltage in response to the first voltage and the current such that the second voltage is positively offset relative to the first voltage (capacitors Cp and Cn in conjunction with transistors M3 and M8)", and "an inverter circuit that includes a p-type transistor and an n-type transistor...(M1 and M2 in Circuit 11)".

With respect to claim 12, the definition of the term "resistor" includes "A device used to control current in an electric circuit by providing resistance" (The American Heritage Dictionary of the English Language, Fourth Edition, 2000). Almost every component in a circuit provides a resistance that limits current, therefore it is reasonable to interpret capacitors Cp and Cn, or even any of the transistors in circuit 10 of Fig. 2 as resistors.

With respect to claim 13, the recited "capacitor circuit" would read on capacitors Cp and Cn.

With respect to claim 14, "the capacitive circuit enables an effective supply voltage that is greater than a relatively smaller supply voltage (the bootstrapped configuration of Cp and Cn in Fig. 2 creates a larger effective supply voltage)."

With respect to claim 15, the increase in "operation speed" discussed in lines 21-30 of col. 1 of Kong et al. will inherently provide the recited operation of reduced propagation delay.

With respect to claim 16, it is well know in the art that the switching of current through a capacitor causes a voltage ramp. This is situation is disclosed in Kong et al., when the voltage supply changes from a high to low value. This causes capacitor Cp in Fig. 2 to become a voltage ramp that differs from the voltage ramp that would occur in Cn, as they would be opposite in magnitude.

With respect to claim 17, Kong et al. discloses, in Fig.2, a circuit comprising: "a means for a logic circuit (M1 and M2) including a p-type transistor (M1) and an n-type transistor (M2)"; and "a means for a voltage offset circuit (remainder of circuit) that is arranged to provide a first voltage to a gate of the p-type transistor, and further arranged to provide a second voltage to a gate of the n-type transistor such that the second voltage is positively offset relative to the first voltage". Kong et al. discloses a voltage offset through using bootstrap capacitors Cp and Cn. First the capacitor Cp and Cn create a boosted effective control signal opposite in polarity. Additionally in both situations of a high or low

input (IN) voltage, M2's gate voltage is positively offset to that of M1's. (See Kong et al. col.2 lines 15-67 and col. 3 lines 1-30.)

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Iketani et al. (USPN 6,229,365) discloses a CMOS circuit arranged as an inverter, and a voltage offset as described in Applicant's first claim.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571) 272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
06/13/05

Terry D. Cunningham
Primary Examiner